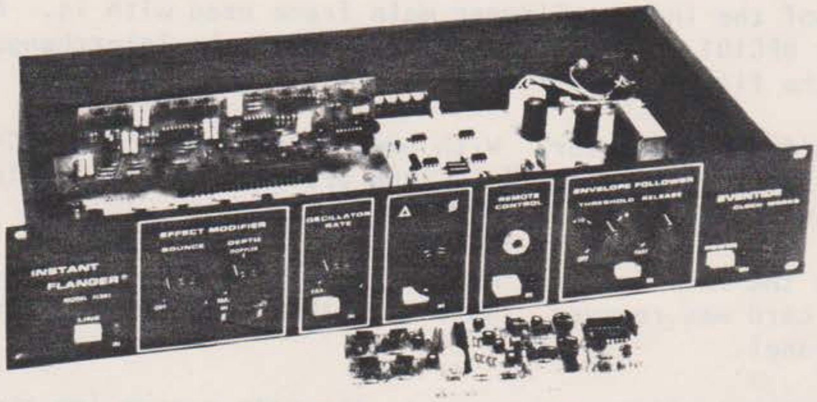
Eventide
the next step

BPC101 PHASER CARD



SPECIFICATIONS

FREQUENCY RESPONSE	Limited primarily by the low-pass filter which precedes the card on the Instant Flanger main frame. The filter has a cut-off frequency of approx. 14 kHz.
DYNAMIC RANGE	Greater than 90 dB, clipping to noise floor.
NUMBER OF PHASE-SHIFT STAGES	Twelve identical stages, auxiliary output tapped from the eighth stage.

FIELD ADJUSTMENTS NECESSARY FOR USE

For proper operation, the BPC101 card must be adjusted to match the characteristics of the individual Instant Flanger with which it is being used. Details of these adjustments are in the USER ADJUSTMENT section below. No changes to the Instant Flanger main frame are necessary, and the original SDC-1 flanger plug-in card may be reinstalled at any time for a return to the Instant Flanger.

NOTE: If you order a Flanger main frame and BPC101 card from Eventide simultaneously, these adjustments will have been made at the factory.

WARRANTY

The BPC101 Phaser Card is warranted for one year, parts and labor (see Instant Flanger Warranty for fuller details). If you return the card for repair, enclose a copy of the sales invoice to substantiate date of purchase.

BE SURE TO ATTACH THIS ADDENDUM TO YOUR INSTANT FLANGER MANUAL FOR FUTURE REFERENCE

EVENTIDE CLOCKWORKS. INC. • 265 WEST 54TH STREET• NEW YORK. N.Y. 10019 • 212-581-9290

USER ADJUSTMENTS

This section describes the calibration of the four variable resistors (trimpots) on the BPC101 Phaser card under three subsections: Calibration to the individual Flanger; Adjustment of the pulse-width modulator; and the trimpot location diagram.

CALIBRATION TO THE INDIVIDUAL FLANGER

It is necessary to adjust the MAIN and AUX trimpots on the BPC101 card to match the characteristics of the Instant Flanger main frame used with it. After this initial calibration, the BPC101 and SDC-1 cards may readily be interchanged, as there are no adjustments to the flanger main frame.

Step 1. Take off the top cover. With power OFF, remove the SDC-1 card. If it is to be stored, wrap it in aluminum foil (the BPC101 card should also be foil-wrapped when stored or shipped).

Step 2. Remove the foil from the BPC101 card and install it in the socket from which the SDC-1 card was removed. Note that the component side of the card should face the front panel.

Step 3. Connect an oscilloscope probe to the main output (on the rear panel terminal strip, MAIN OUTPUT +, or at the test point near the front of the Flanger main circuit board). Alternatively, monitor the output of the unit with an amplifier and speaker (NOTE: keep the volume low at first, to avoid damaging the amp in the event that there is a problem). Apply a 1 kHz tone to the input of the Flanger. Push the LINE switch IN. Set the BOUNCE control fully counter-clockwise, select the MANUAL function only, and set the DEPTH control to MAX OUT.

Step 4. Apply power to the unit. You should see (or hear) the 1 kHz tone at the main output. Rotating the manual control should result in several changes in the amplitude of the output, from a maximum to near-zero. Connect an oscilloscope or an AC voltmeter to the main output. Set the MANUAL control fully counter-clockwise. Now rotate it slowly clockwise to the second minimum reading point (a 'null') and adjust the MAIN pot on the BPC101 card to maximize the depth of the null (i.e., a visible or meter reading of near-full cancellation). The null setting of the MAIN pot will differ for the several nulls that will occur at different points of rotation of the MANUAL control, however, using the setting achieved on the second null as described above will give the optimum average setting.

Step 5. Repeat Step 4 for the auxiliary output, using the AUX pot on the BPC101 card. Note that the nulls are fewer and further apart at the auxiliary output.

This completes the alignment. If you use a small dab of nail polish to secure these settings, the BPC101 and SDC-1 cards may easily be exchanged without readjustment.

The other two pots should not be disturbed unless the FL201/Phaser card combination fails the following test:

a) Set up the unit as in Step 3 above (1 kHz tone in, MANUAL only, observe main output).

b) Listen for four nulls in the output as the MANUAL control is rotated. If there are less than four nulls, or a small 'pop' is heard as the MANUAL control is rotated to the fully clockwise position, then perform the adjustments below.

If the unit passes the test, replace the top cover. The unit is now ready for use.

ADJUSTMENT OF PULSE-WIDTH MODULATOR

The following adjustments must be performed if a component that will affect the operation of the pulse-width modulator is replaced, and may have to be performed upon installation (see previous section). These components include any in the pulse-width modulator circuit itself, either of the two regulator pass transistors, or the associated zener diodes. Adjustment is usually not necessary on initial installation.

Step 1. Use a triggered sweep oscilloscope with a bandwidth of at least 10 MHz. Connect a probe to the pulse-width modulator test point. Connect the ground connection of this probe to the ground test point on the Flanger main board (it is behind the lower left-hand corner of the BPC101 card).

Step 2. Apply power to the Flanger, and allow five minutes for the unit to warm up.

Step 3. Set the front panel controls as follows:

LINE	IN
BOUNCE	Fully counter-clockwise
DEPTH	Any setting
OSCILLATOR	Any setting
MANUAL	Fully counter-clockwise
ENVELOPE FOLLOWER THRESHOLD	Any setting
ENVELOPE FOLLOWER RELEASE	Any setting

Select only the MANUAL control. All the function select pushbuttons should be OUT except for MANUAL.

Step 4. Observe pin 6 of IC K. The repetition frequency of this waveform should be approximately 100 kHz. If it is less than 80 kHz, install a resistor (typical value would be 20 k - 50 k) in parallel with that directly under IC K. If it is greater than 120 kHz, install a capacitor (typical value would be 50 pF to 500 pF) in parallel with that directly under IC K.

Step 5. With the MANUAL control set fully counter-clockwise, the MIN pot should be set so that the pulse width is 500 ns (time the signal is low), as observed at the test point.

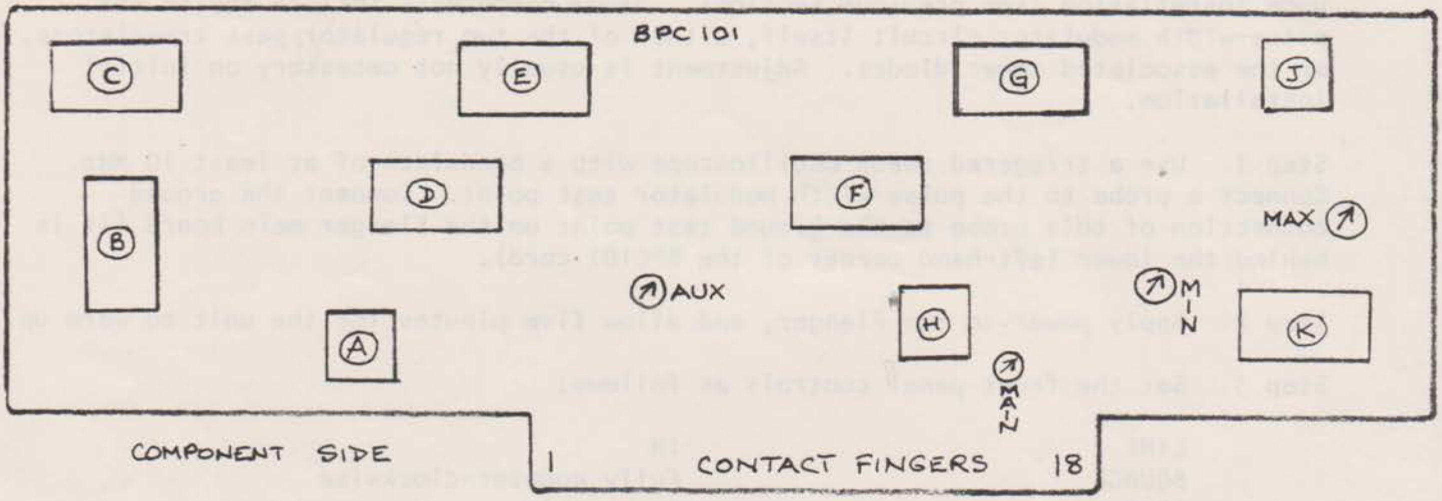
Step 6. Rotate the MANUAL control fully clockwise. Adjust the MAX pot for a pulse width of 300 ns (time when the signal is high), as observed at the pulse-width modulator test point.

Step 7. Repeat Steps 5 and 6 until the pulse-widths are as noted. Repetition is necessary as the two controls interact.

Step 8. Re-check the pulse-width variation. It should vary from 500 ns low to 300 ns high as the MANUAL control is rotated from fully counter-clockwise to fully clockwise.

Step 9. Seal the MIN and MAX pot adjustment with nail polish. This ends the pulse-width modulator adjustment procedure.

TRIMPOT LOCATION DIAGRAM



THEORY OF OPERATION

Phasing, like flanging, is an effect produced by mixing a direct signal with a delayed signal. Flanging employs an actual time delay; phasing uses variable phase-shift networks. The primary difference is that a phase-shift network has a different amount of delay at different frequencies. Previous designs have used Field Effect Transistors operating in the linear mode as variable resistors, which severely limited the dynamic range of the phaser. The BPC101 avoids the problems of poor dynamic range and the necessity for device matching that plagued earlier phasers.

The variable resistance used in this design is of FET-type construction, but operates in a switched mode rather than in a linear mode, to eliminate the problems of the linear approach. The specific device used is a bi-directional analog switch or transmission gate (The CD4066 quad device manufactured by National Semiconductor, RCA, and others). Since these devices need not be matched, they can easily be replaced, should this ever be necessary.

A transmission gate can be made to act as a variable resistor by switching it on and off rapidly and controlling its pulse width, i.e., the ratio of its ON time to OFF time. The wider the pulse width, the lower the average resistance. The BPC101 card substitutes a pulse-width-modulated transmission gate for a resistor in a phase-shift network (see schematic) to achieve wide dynamic range (the signal can swing between the supply rails). There is no component matching necessary, and the useful range of the pulse-width modulation is 95%.

The on/off nature of the operation used is identical to that of sampling. There are two effects of concern; aliasing and resolution. Resolution (quantizing error) is not a problem, since the signal is not actually converted from analog to digital. For the same reason, there are no speed constraints placed on the system, and so the sampling rate can be placed so high that aliasing is of no concern. However, we have provided input and output low pass filters to avoid any possibility of spurious signal outputs.

DESCRIPTION OF CIRCUITRY

All inputs and outputs to and from the card, as well as the power supply connections, are through the 18-pin edge connector at the base of the card. All the connections are on the rear of the card. The pins used are detailed in the schematic.

The audio input proceeds to an inverting amplifier (IC A) with a gain of approximately 3. This boosts the audio level, following the attenuation of the SDC level pot on the Flanger main frame, the better to utilize the dynamic range of the following circuitry. Next, the audio signal goes through a two-pole low pass filter with a cutoff of about 15 kHz (IC A). From this point, the signal goes to the phase-shift networks of IC's B through G. These six IC's are used in identical circuits, in which the variable resistance element is a pulse-width-modulated transmission gate.

The output of each phase-shift network is noted on the BPC101 card by a small number at the output of each stage's op amp. At the eighth- and twelfth-stage outputs, there are low-pass filters (IC H) identical to the input filter (to remove any HF noises which might interfere with the following circuitry), and a series pot to allow custom adjustment of the mix of phase-shifted and direct signals at the main and auxiliary outputs. There is also a high-pass filter to remove the small offset that develops on the card due to clock feedthrough in the gates. This is formed by the DC blocking capacitor in series with each filter output. Each of these filters has a cutoff of approximately 40 Hz.

PULSE-WIDTH MODULATOR

The pulse-width modulator includes IC's J and K on the right-hand side of the card. IC J is a high-speed comparator; an LM710CH. IC K is another quad transmission gate; a CD4066.

The method used here compares the control voltage signal generated on the Flanger main board with a sawtooth or ramped voltage. Due to the characteristics of a comparator, whenever the voltage level of the ramp is greater than the voltage level of the control voltage, the output of the comparator will be at low level, and vice versa.

The CD4066 is used as a free-running oscillator, and as the charging mechanism for the capacitor on which the ramp is generated. Its operation is as follows: at turn-on, the .001 uF capacitor charges through the 4.7 k resistor. When the voltage at pin 6 (the control pin for the transmission gate of pins 8 and 9) reaches the positive-going CMOS threshold voltage, a series of events occurs. First, the 8, 9 transmission gate (TG) closes (low impedance state), and the control inputs for TG 1, 2 (pin 13), and TG 10, 11 (pin 12) are brought to a 12 volt potential. The 1 k resistor pulls the voltage back to ground level when TG 8, 9 is open (high impedance state). TG 1, 2 impresses a charging voltage on the delay circuit of the 15 k and 82 k resistors and the 100 pF capacitor. When the voltage at pin 5 (the control input for TG 3, 4) reaches the CMOS threshold, TG 3, 4 closes and discharges the .001 uF capacitor. This causes TG 8, 9 to open, and the voltage at pins 12 and 13 returns to 0 V. TG 1,2 now opens and allows the voltage at pin 5 to fall below the CMOS threshold due to the action of the 82 k resistor, thus opening TG 3, 4. The .001 uF capacitor is no longer grounded and begins to charge again, repeating the cycle. This oscillator operates at a rate of over 100 kHz.

The function of TG 10,11 is to charge up the ramping capacitor. This is continually discharged towards -15 V by the constant current source composed of a 2N3391 transistor and its associated variable emitter resistance. The capacitor cause a complete lack of output, unless it shorts internally to one of the power supplies. If a phase-shift stage is operating (and the associated transmission gate is being clocked), the signal - assuming a 1 kHz sine wave input to the Flanger - should appear at the non-inverting op amp input for each stage as a sine wave whose amplitude decreases as the MANUAL control is rotated clockwise (MANUAL button IN, all others OUT, BOUNCE OFF). Each phase-shift stage has unity gain.

AUDIO OUTPUT PRESENT, BUT NO OR INSUFFICIENT PHASING

With only the MANUAL control operative, BOUNCE OFF, and a 1 kHz sine wave input, there should be at least four nulls from the main output. If there are none, the pulse-width modulator is probably not working. If there are one, two or three nulls, either the pulse-width modulator needs adjustment or there are one or more bad transmission gates (see the end of the USER ADJUSTMENTS section for the method of testing each phase-shift section).

If the pulse-width modulator is not working, check: a) the free-running oscillator, b) the current sink transistor and ramping capacitor, c) the comparator, d) the diode level shifter. Waveforms for the pulse-width modulator are shown with the schematic drawings.

A 'POP' IS HEARD AT MAXIMUM PHASE SHIFT (when LED on front panel is fully lit)

The pulse-width modulator is not aligned properly, i.e., the duty cycle of the pulse-width modulator can go to 0% (always a low logic level). Perform the pulse width adjustment outlined in the USER ADJUSTMENTS section.

AUDIO BREAKUP WHILE PHASING

A transmission gate may be defective, or its operating point may have shifted. Locate the failure by tracing through the phase-shift stages. Before replacing any parts, try shorting one of the diodes of the diode level shifter.

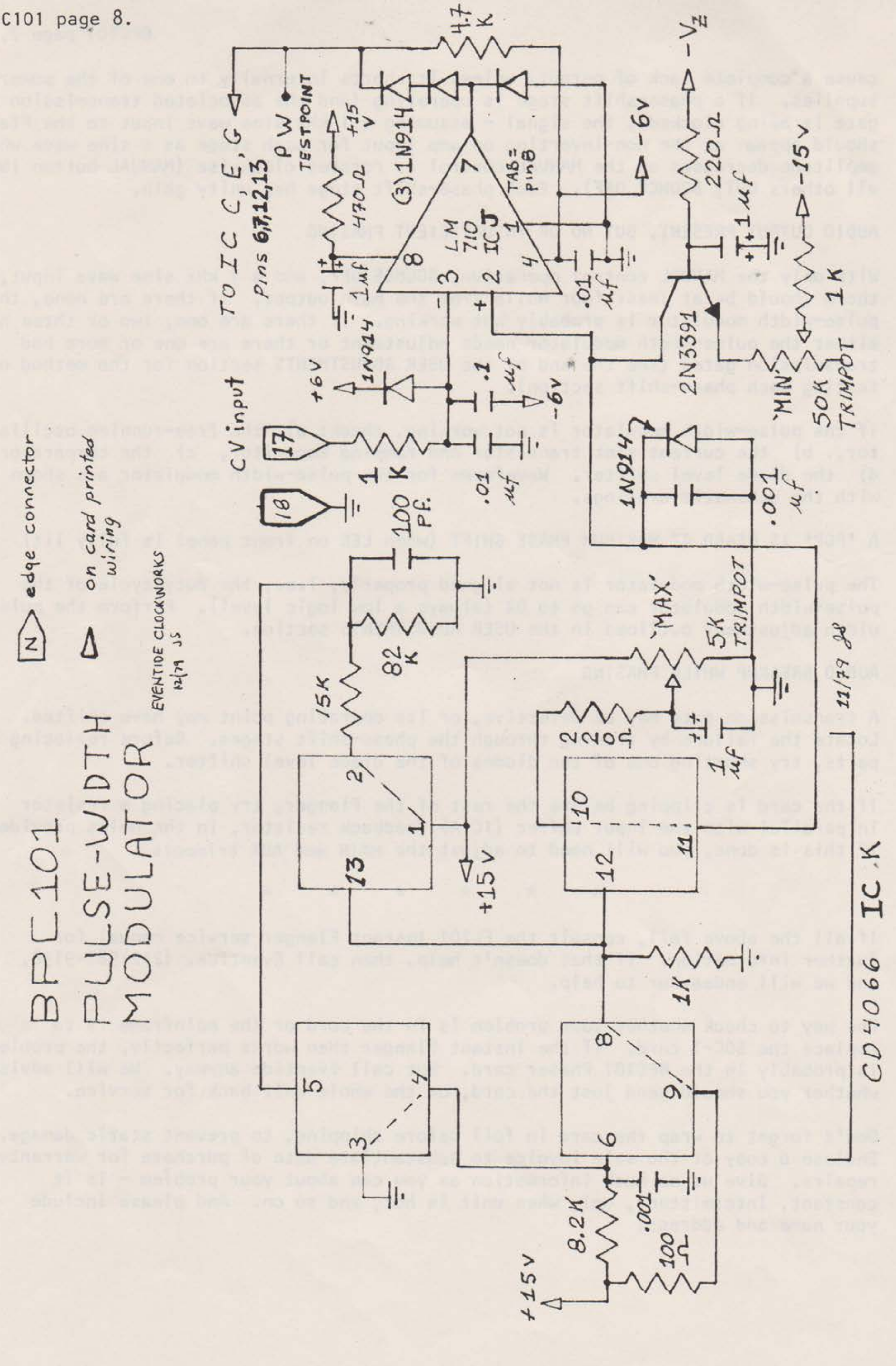
If the card is clipping before the rest of the Flanger, try placing a resistor in parallel with the input buffer (IC A) feedback resistor, in the holes provided. If this is done, you will need to adjust the MAIN and AUX trimpots.

* * * * * *

If all the above fail, consult the FL201 Instant Flanger service manual for further information. If that doesn't help, then call Eventide, (212)581-9138, and we will endeavour to help.

One way to check whether your problem is in the card or the mainframe is to replace the SDC-1 card. If the Instant Flanger then works perfectly, the problem is probably in the BPC101 Phaser card. But call Eventide anyway. We will advise whether you should send just the card, or the whole unit back for service.

Don't forget to wrap the card in foil before shipping, to prevent static damage. Enclose a copy of the sale invoice to substantiate date of purchase for warranty repairs. Give us as much information as you can about your problem - is it constant, intermittent, only when unit is hot, and so on. And please include your name and address!


BPC101
PULSE-WIDTH
MODULATOR
EVENTIDE CLOCKWORKS
12/79 JS
N edge connector
on card printed wiring
CV input
TO IC C, E, G
pins 6,7,12,13
PW
TESTPOINT
(3) 1N914
+15 V
470 Ω
LM 710
IC J
TAB = PIN 8
1N914
+6V
-6V
.01 µf
.1 µf
1 µf
100 pF
1 K
82 K
15K
4.7 K
-V_Z
220 Ω
-15 V
2N3391
1N914
.001 µf
'MIN'
50K
TRIMPOT
1 K
'MAX'
5K
TRIMPOT
1 K
+15 V
8.2K
.001
100 Ω
1 µf
2.2K
CD4066 IC K
11/79 JS

voltage is prevented from going negative by the diode connected in parallel with it. The network composed of the MAX pot, the 1 uF capacitor, and the 220 ohm resistor connected to pin 10 of IC K determines the maximum value of the voltage that will be applied to the ramping capacitor when TG 10,11 is closed. The MAX pot's wiper can have a voltage between 0 and 15 V. This is stored on the 1 uF capacitor, which acts as a reservoir. The 220 ohm resistor acts as a current limiter.

The system outline above applies a pulse of current to the ramping capacitor, the voltage of which is linearly run down to 0 V by the the constant current source. The MIN pot (the adjustable emitter resistance of this transistor) permits adjustment of the time it takes for the voltage to run down. This does not affect the frequency of the free-running oscillator.

Finally, the ramp voltage is compared to the control voltage signal from the Flanger mainframe by the LM710 (IC J), and as long as the ramp is greater than the control voltage, the output is high, keeping the TG's in the phase-shift networks closed. The diode level-shifter circuit offsets the output of the LM710 to fit the bipolar signal excursion necessary for the phase-shifter TG's to work properly, since they operate on a bipolar supply.

The MAX pot sets the peak voltages of the ramp, thus setting the minimum pulse width when the control voltage is at its maximum value of about 7 volts. The MIN pot determines the slope of the ramp, thus fixing the maximum pulse width when the control voltage is at 0 V. MIN and MAX therefore refer to the ramp voltage waveform, and only indirectly to the pulse width. These adjustments are interactive; you cannot change one without changing the other.

POWER SUPPLY

The Flanger mainframe provides ± 15 volts. the +15 and -15 V supplies are used directly by IC H. The +15 V is used by the pulse-width modulator. The rest of the circuit operates from regulated ± 6 volt supplies, each composed of a zener diode with its appropriate current-limiting resistor, and a medium power series pass transistor. This allows the transmission gates to operate on a bipolar supply. There are 'fuse' resistors at the +15 and -15 V inputs and after each regulator. These must be replaced, if necessary, with the correct type (¼ watt, 4.7 ohms).

TROUBLE-SHOOTING HINTS

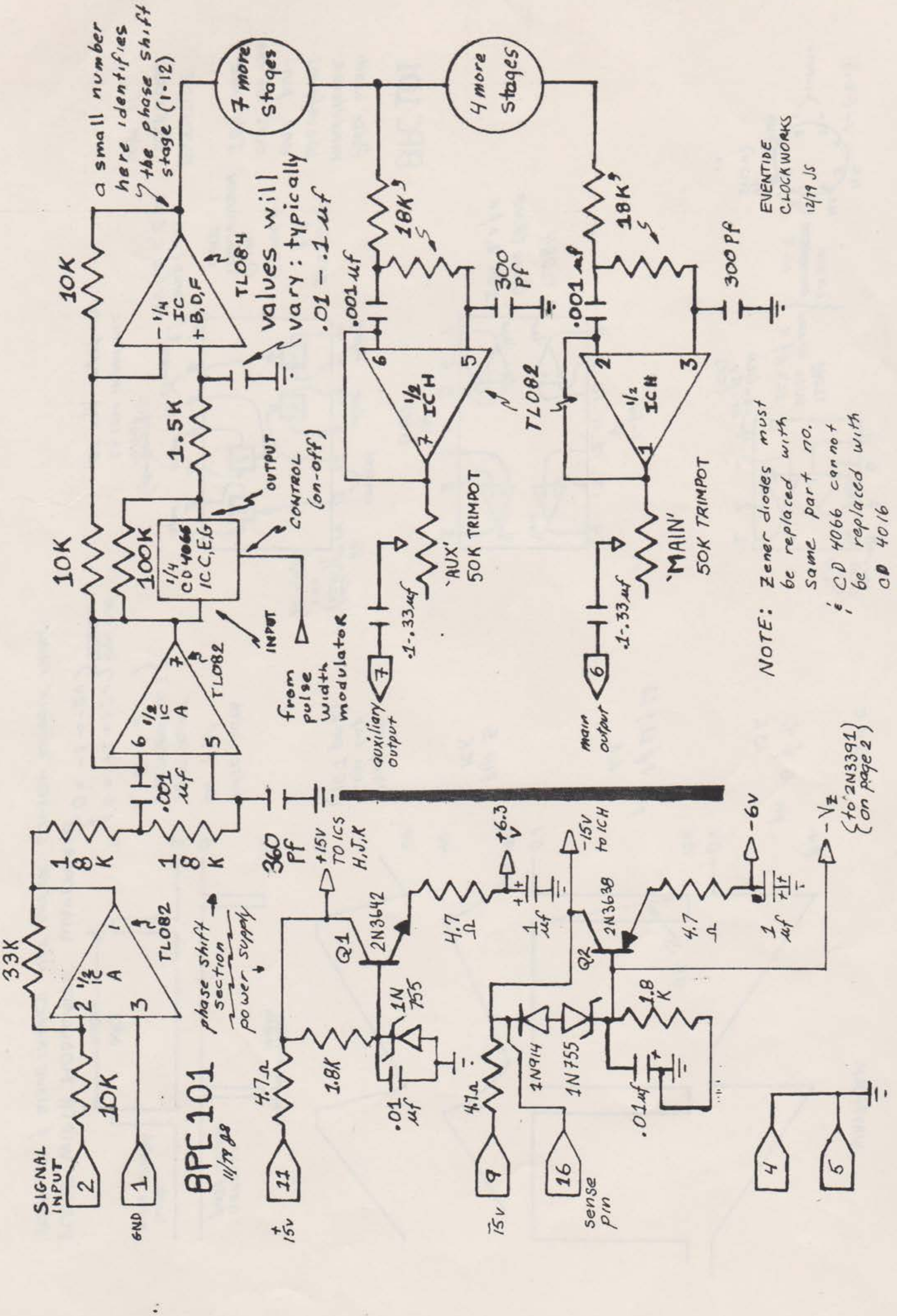
NO AUDIO OUTPUT FROM CARD (either Main or Auxiliary Output)

1. Check the on-card power supplies. If one or both voltages are missing, check a) the Flanger mainframe power supply, b) the on-card regulators, and c) the ±15 V circuitry on the card (output filters and pulse-width modulator). NOTE that the fuse resistors will probably burn if there is a short circuit, and should be replaced with the same type (¼ watt, 4.7 ohms). A bad bypass capacitor is a possibility, and is more probable than a bad IC.

2. Check the input buffer amp and filter.

3. Trace through the phase-shift sections one by one. The stage numbers are marked at each corner of the quad op amps.

4. Check the output filters and trimpot circuit. You can see the card outputs at the test points on the Flanger main board directly in front of the card (main on right). If a problem is found in any phase-shift stage, there are several possibilities: a) an open-circuit phasing capacitor, b) a bad op amp stage, c) a broken resistor or open trace. It is fairly unlikely that a bad transmission gate will


BPC 101
11/78 JS
phase shift section
power supply
SIGNAL INPUT
GND
+15v
-15v
sense pin
10K
33K
TL082
1/2 IC A
1.8 K
.001 uf
360 pf
1/2 IC A
TL082
10K
100K
1/4 CD 4066 IC C,E,G
INPUT
OUTPUT
CONTROL (on-off)
from pulse width modulator
1.5K
10K
-1/4 IC +B,D,F
TL084
values will vary: typically .01 - .1 uf
a small number here identifies the phase shift stage (1-12)
7 more Stages
4 more Stages
.001 uf
18K
300 pf
1/2 ICH
TL082
'AUX' 50K TRIMPOT
'MAIN' 50K TRIMPOT
.1-.33 uf
auxiliary output
main output
+15V TO ICS H,J,K
Q1
2N3642
1N 755
4.7 Ω
1 uf
+6.3 V
-15V to ICH
Q2
2N3638
1N914
1N755
1.8K
.01 uf
-6V
-Vz
(to 2N3391 on page 2)
NOTE: Zener diodes must be replaced with same part no.
CD 4066 cannot be replaced with CD 4016
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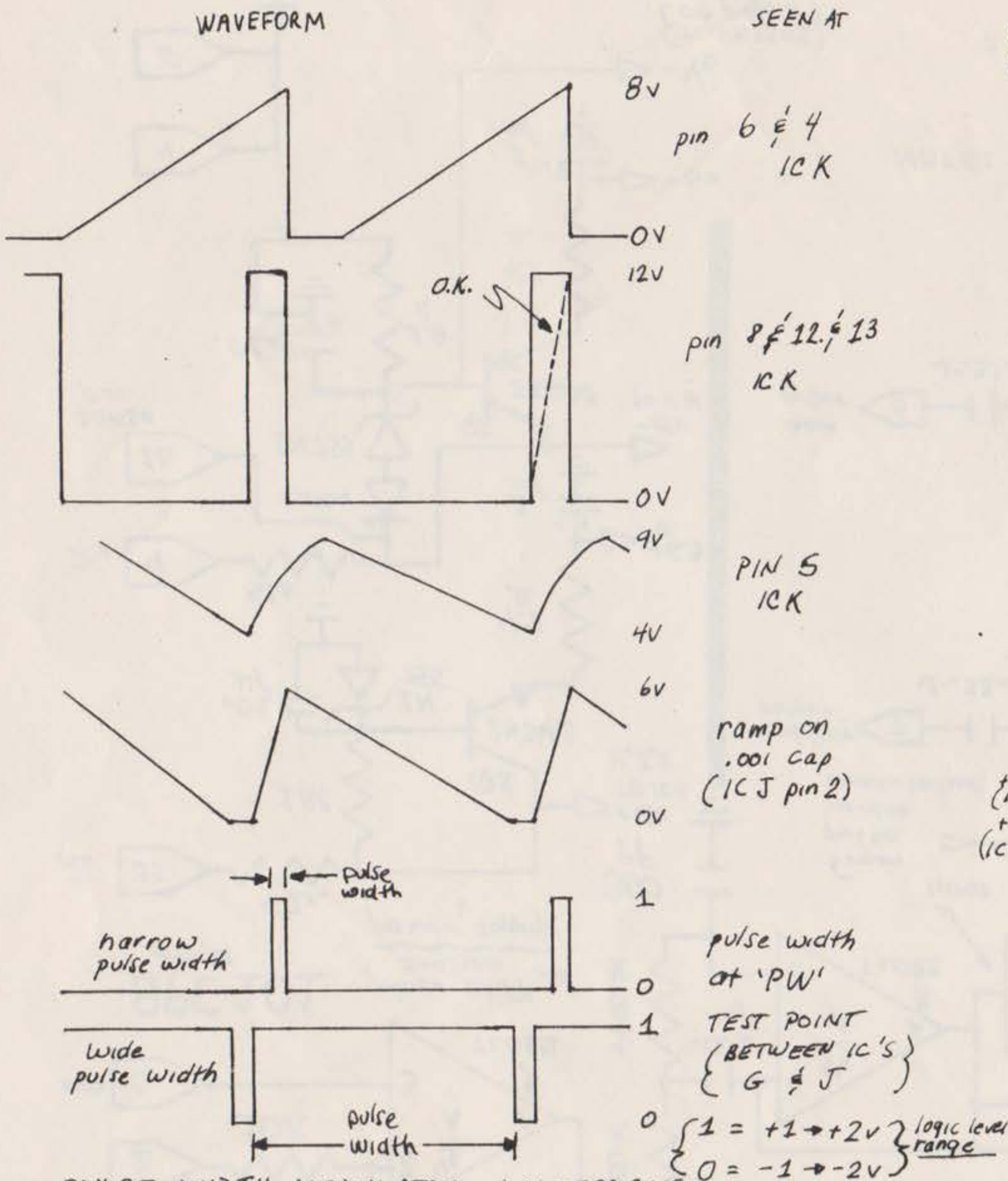
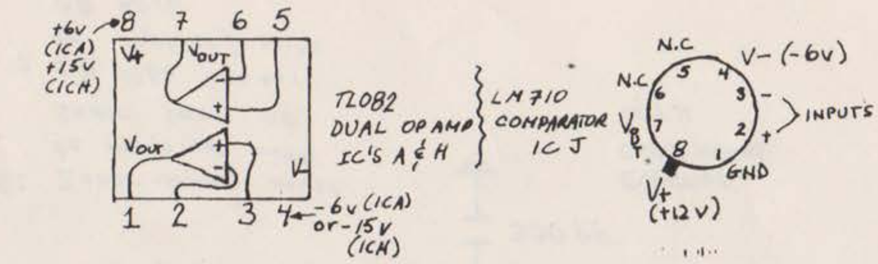
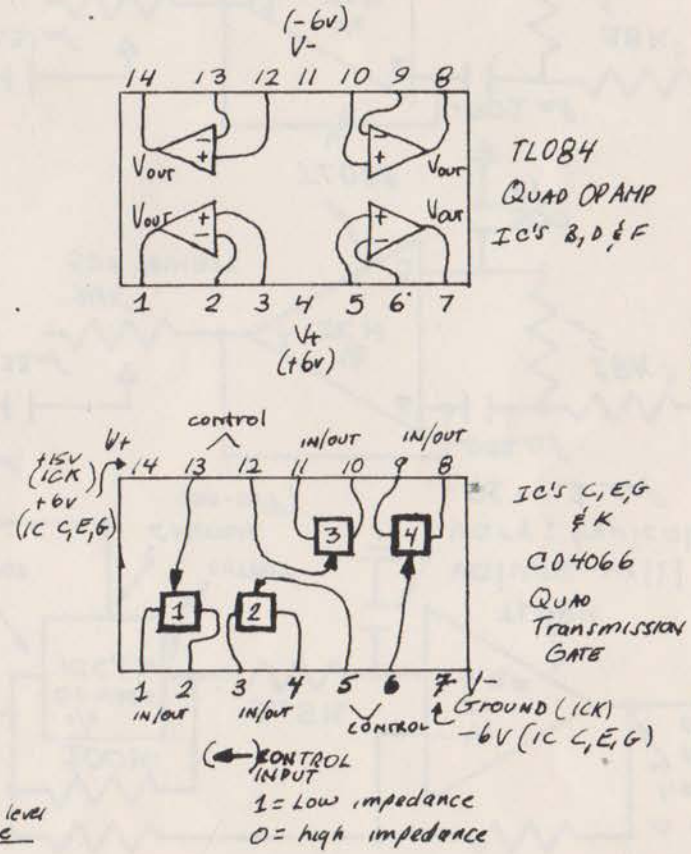


PULSE WIDTH MODULATOR WAVEFORMS
VOLTAGES & WAVESHAPES MAY DIFFER SLIGHTLY WITHOUT FAULT





BPC 101

Pulse width modulator waveforms and pin-outs of the IC's used

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